Hodoscopic CsI Calorimeter Electronics Design Status

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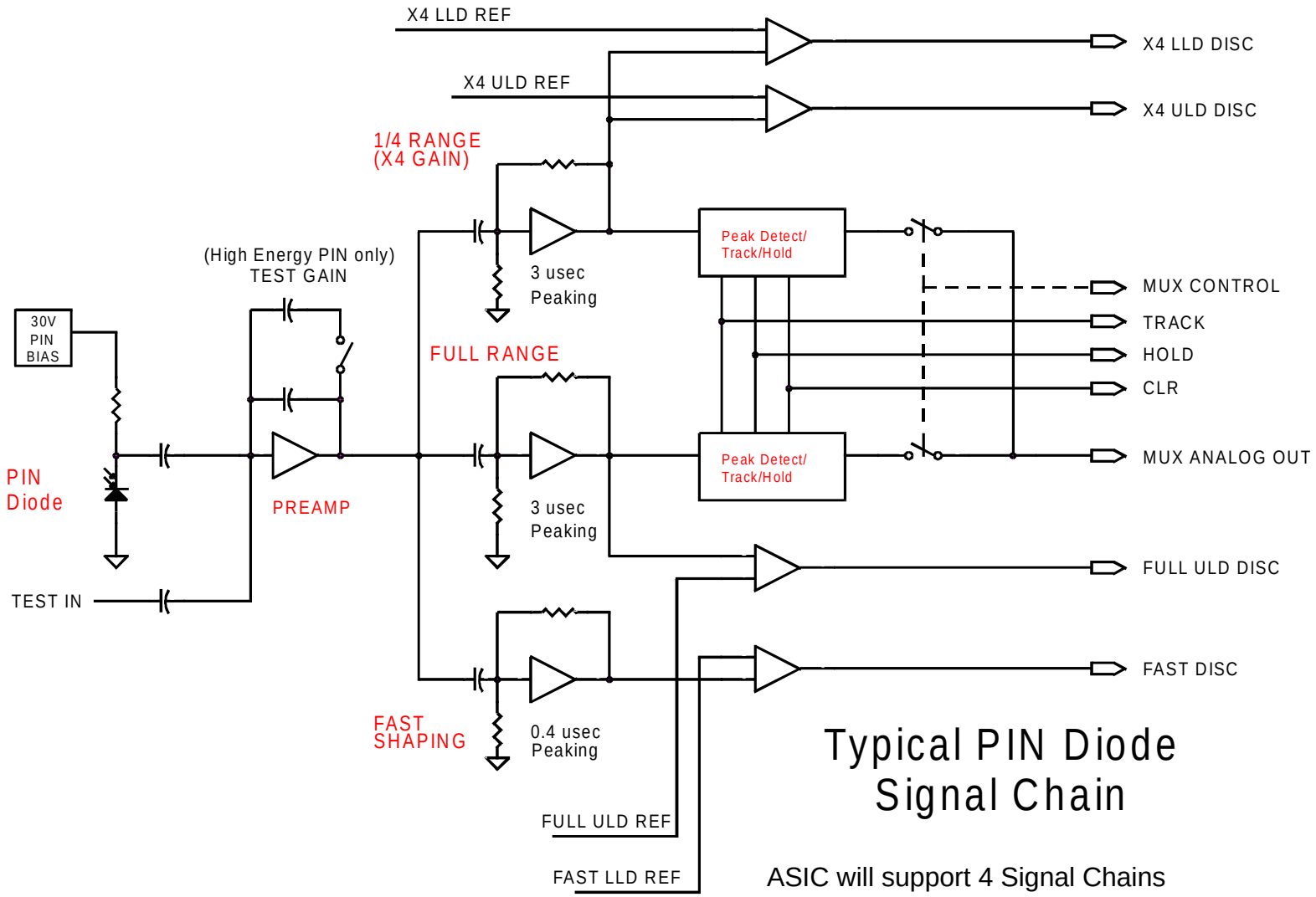
10 February 1998

Prototype ASIC

- Design requirements reviewed by NASA/GSFC (Satpal Singh, Don Stillwell), NRL, UCSC (David Dorfan)
- Design and simulations by Satpal Singh (Prime Circuits Inc./GSFC)
- Prototype in HP 0.5 μm process.
- Design submitted to MOSIS on Dec 19, 1997. Prototype Parts available late March, 1998
- Preamp and Shaping Amp for both gain ranges - 2 PIN diodes
- Each preamp will feed two shaping amps with slightly different ranges. Total of 4 shapers, discriminators and peak-detect/holds per CsI block end. (Concern is dynamic range of peak detect signal).
- Discriminator thresholds set by external reference voltages (rather than DACs in full design)
- Each of the 4 channels is processed via mux by 10/12-bit ADC (perhaps ASIC)
- Prototype ASIC supports 4 PIN diodes (2 complete channels and 2 full range only channels)

Protoype ASIC PIN Signal Chain



Typical PIN Diode Signal Chain

ASIC will support 4 Signal Chains
- 2 low gain and 2 high gain.

Prototype ASIC Channels

High Gain Channel

- 0 - 320 MeV Nominal Energy Range
- Hamamatsu S3590-01 PIN diode (1 cm^2)
  - collects 10^4 e^-/MeV (1.6 fC/MeV)
  - C_{diode} = 80 pF
- Required gain is ~ 6 mV/fC
- Preamp
  - 1 pf feedback capacitor = 512 mV full scale
- Shaping Amps
  - full range, 3 μsec peak, gain ~ 6
  - 1/4 range (X4), 3 μsec peak, gain ~ 24
  - fast shaping, 0.4 μsec peak, gain ~ 60

Low Gain Channel

- 0 - 40.96 GeV Nominal Energy Range
- Custom PIN Photodiode (0.25 cm^2)
  - collects 2500 e^-/MeV (0.4 fC/MeV)
  - C_{diode} = 30 pF
- Required gain is ~ 180 μV/fC
- Preamp
  - 15 pf feedback capacitor = 1.1 V full scale
- Shaping Amps
  - full range, 3 μsec peak, gain ~ 3
  - 1/4 range (X4), 3 μsec peak, gain ~ 12
  - fast shaping, 0.4 μsec peak, gain ~ 30

Prototype ASIC Discriminators

Each PIN diode has 4 discriminator outputs:

- FULL ULD - Fixed upper level disc on Full Range used for ADC gain range selection by controlling FPGA.
- X4 ULD - Fixed upper level disc on X4 Range used for ADC gain range selection by controlling FPGA.
- X4 LLD - Programmable lower level disc on X4 Range used for track/hold signalling to controlling FPGA
- FAST LLD - Programmable Fast Shaping lower level disc used for calorimeter triggers into GLAST trigger controller.

Prototype ASIC Shaping Amps

- Two shaper gains per PIN diode and preamp (3 usec peaking)
- Differ in gain by approximately x4.
- *Will test performance and return to one gain per PIN if dynamic range can be achieved in one shaper - peak detect per PIN.*
- One fast shaper (0.4 μsec peaking) per PIN

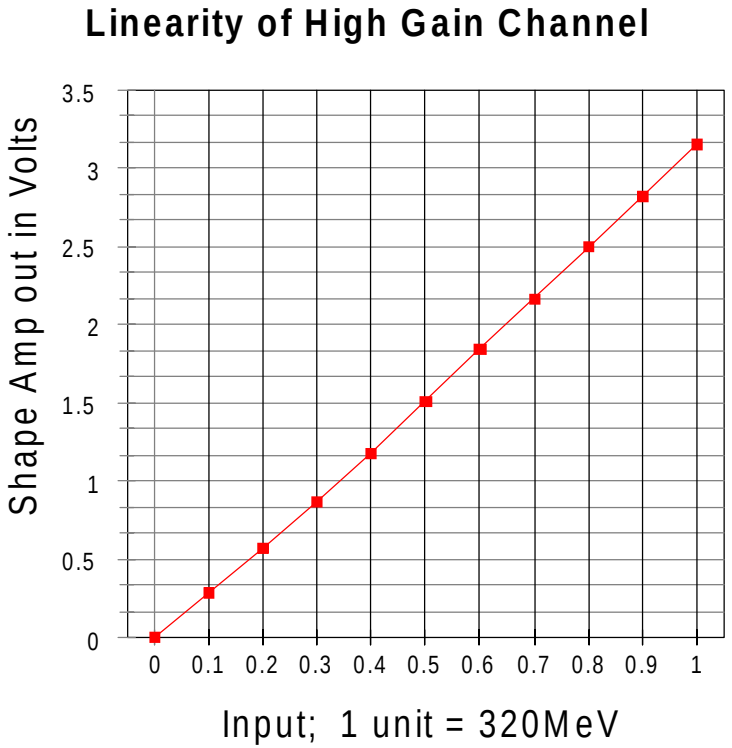
	High Gain X4	High Gain Full	Low Gain X4	Low Gain Full	Low Gain Fast Shaping
Max Energy	80 MeV	320 MeV	10.24 GeV	40.96 GeV	40.96 GeV
Chan Width	0.078 MeV	0.312 MeV	10 MeV	40 MeV	n/a
Threshold	1 MeV	80 MeV	300 MeV	10 GeV	~ 1 GeV
Noise Estimate (Simulation)	1500 e^- rms (0.15 MeV)	1200 e^- rms (0.12 MeV)	13,500 e^- rms (5.4 MeV)	8000 e^- rms (3.2 MeV)	2×10^5 e^- rms (80 MeV)
Quantization Error @ Thresh	8%	0.4%	3%	0.4%	n/a
Chan # of 1 MIP	256/1024	64/1024	2/1024	0	n/a
Chan # of ^{12}C	**	**	72/1024	18/1024	(~9 × noise)

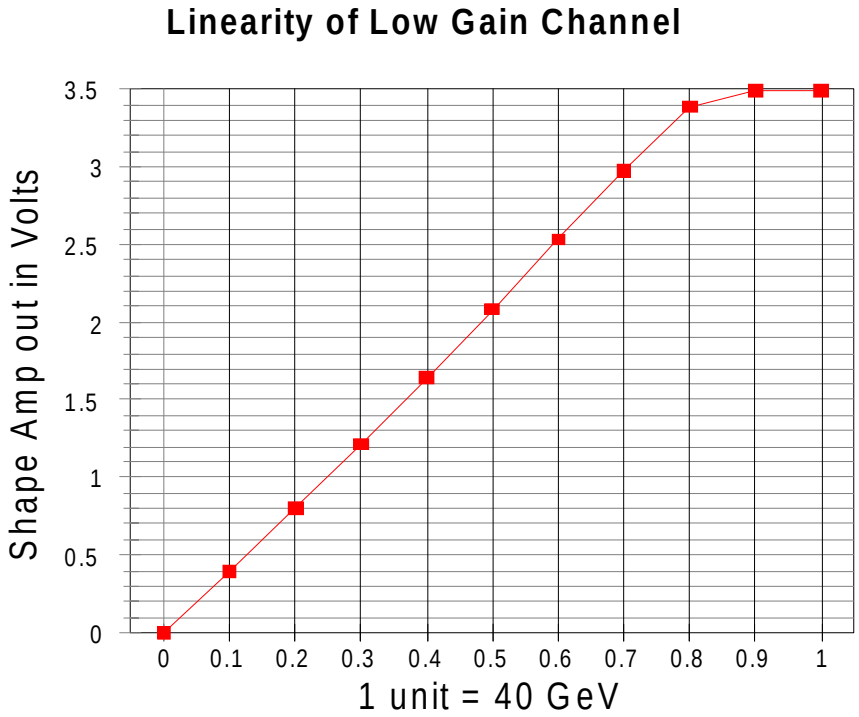
ASIC Power/PIN Estimate

	Quantity	Power/ea (μW)	Power/chan (μW)
Preamp	1	130	130
Shapers	3	25	75
Peak Detect	2	35	70
Discriminators	4	35	140
TOTAL / PIN			**415 μW**

ASIC Power / GLAST Tower = 80 x 4 x 415 = 133 mW

ASIC Simulations
Linearity

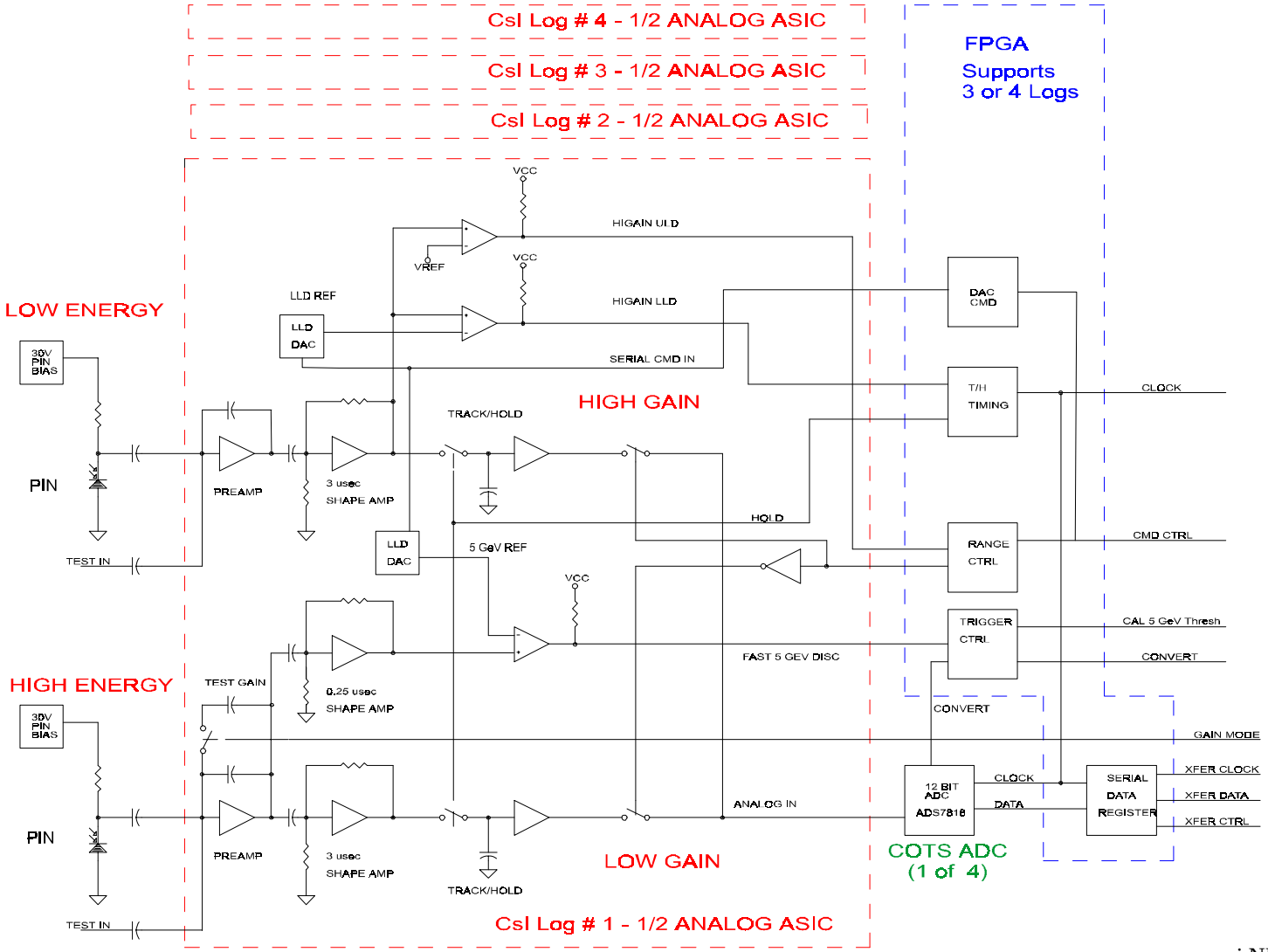




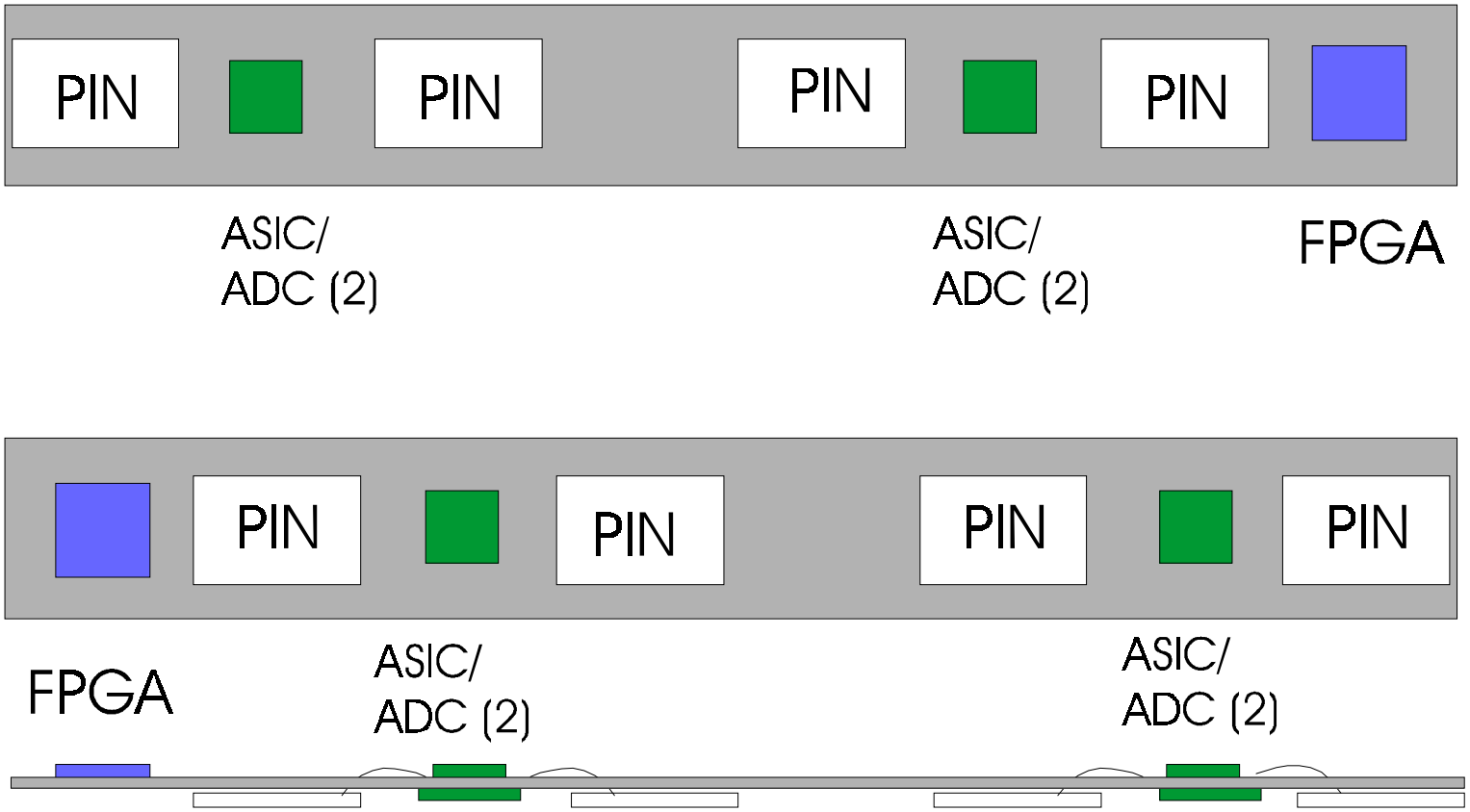
ASIC Development
Future Work

- Prototype parts received in March, die testing by GSFC
- Prototype die will also be tested by UCSC
- NRL will mount and bond die into ceramic leadless chip carriers for board testing.
- NRL has designed printed circuit board for testing ASIC with potential COTS ADCs
  - interface to pulsers or PIN diodes
  - logic contol via Xilinx FPGA
  - COTs ADCs from Burr Brown, Maxim, and Analog Devices
  - optical isolation for readout to test computer.
- Next prototype will include
  - serial command communications,
  - programmable DACs for discrimination references,
  - programmable test charge injection,
  - commandable discriminator enable/disable

Calorimeter
Front End Electronics Concept



Calorimeter Front End Circuit Card Concept



Calorimeter Electronics Organization